SEMICONDUCTORS

**New name for Electrical Characterization Metrology project.

Office of Microelectronics Programs

Office Director: Robert I. Scace

Staff: 3 professionals (1 physicist, 1 physical chemist, 1 secretary)

Funding level: $10.4 million (as of end FY 1996)

Funding sources: NIST

Objective: Develop and execute NIST's National Semiconductor Metrology Program (NSMP); apply NIST-wide technical resources regardless of organizational location to deliver solutions to highest priority metrological problems of the semiconductor industry. Provide formal liaison to SEMATECH and the Semiconductor Research Corporation.

Background: NIST has developed metrology for the semiconductor industry for over 40 years in EEEL and its predecessors. Ten years ago, the breadth of technology then applied in semiconductor manufacturing clearly transcended EEEL's technical scope. New appropriated funds were sought, and first obtained in 1991. The Semiconductor Industry Association (SIA) took the initiative in defining and gaining Administration support for the National Semiconductor Metrology Program, established in early 1994. The needs are identified in the National Technology Roadmap for Semiconductors, the third in a series of needs documents developed with strong industry participation led by the SIA. The technical program is confined by agreement to mainstream digital silicon complementary metal oxide-semiconductor (CMOS) technology.

Current Tasks (Listed below are NSMP-funded tasks in other NIST organizations. NSMP-funded tasks within EEEL's domain are described elsewhere in this document)**:**

1. Dimensional Metrology at the Nanometer Level

FY 1995	Developed calibrated atomic force microscope (C-AFM); Procured high resolution field emission scanning electron microscope (FESEM) and compatible scanning probe microscope (SPM) for combined metrology system.
FY 1996	Completed initial characterization of the C-AFM performance for pitch, height, and width measurements; Completed initial measurements of silicon single atom step height specimens; Completed installation and initial optimization of both the FESEM and the SPM; Provided first-order feedback to the manufacturers of both of these instruments regarding the functioning of the combined instrumentation system.
FY 1997	Complete top width measurements of preferentially etched silicon sample for the linewidth measurement comparison; Procure prototype specimens for a combined pitch/height standard reference material; Optimize the current SPM for operation in the FESEM in collaboration with the manufacturer; Perform combined SEM/SPM scans of the SEM sharpness standard and RM 8090.

FY 1998 Certify the C-AFM as a NIST calibration facility and perform first calibrations; Disseminate silicon single atom step specimens for trials by collaborators; Design and collaborate in the manufacture of a combined SEM/SPM which optimizes the strengths of both systems.

2. Plasma and CVD Process Measurements

FY 1995 Demonstrated utility of radio frequency (rf) measurements to monitor polymer build-up in plasma reactors; Modified Gaseous Electronics Conference (GEC) rf Reference Cell to accept inductively coupled plasma source; Measured/published spatial distribution of carbon-fluorine (CF) radicals in carbon tetrafluoride/oxygen/argon plasmas.

FY 1996 Performed critical review of available electron collision data for carbon tetrafluoride (CF_4) and trifluoromethane (CHF_3) and constructed World Wide Web-based database; Transferred rf electrical measurement techniques (hardware and software) to a specialty gas supplier and began investigation of electrical properties of nitrogen trifluoride (NF_3) discharges; Measured electron density and energy distribution functions in the inductively coupled plasma source for wide range of gases and plasma conditions; Measured first time-resolved optical emission spectra of rf biased electrode sheaths in inductively coupled plasma reactor.

FY 1997 Extend electron impact database of plasma processing gases to include Dichloro-difluoromethane (CCl_2F_2), perfluoroethane ($C_2F_{6)}$, and perfluoropropane (C_3F_8); Publish studies (in collaboration with gas supplier) of electrical characteristics and power coupling efficiency in NF_3 discharges used in deposition reactor cleaning processes; Measure density and temperature profiles for atoms and ions in the GEC inductively coupled plasma source; Investigate the potential of using electron plasma waves for measuring plasma electron densities.

3. Optical CD and Overlay Metrology

FY 1996 Stewart platform strut joint patent approved, licensed to industry; UV linewidth and overlay microscope programming commenced for fully automated instrument control and data acquisition; Major components of overlay system assembled and tested; optical system performance demonstrated on industrially supplied 8" wafer overlay targets.

FY 1997 Complete programming of ultraviolet microscope for pitch calibrations, align and certify it, and calibrate SRM 2800 pitch standards; Align interferometers and qualify overlay metrology system; Manufacture prototype alignment artifacts and measure with the overlay system.

FY 1998 Calibrate 2-dimensional microgrid artifact, and design, manufacture and test conventional (e.g. frame in frame) overlay standard artifact; Complete programming of ultraviolet microscope for calibration of linewidth standards; Extend photomask linewidth standards to 0.25 µm.

4. Fundamental Process Control Metrology for Gases

FY 1995 Developed prototype calibration system for partial pressure residual gas analyzers (RGAs); Developed primary and transfer flow standards for inert

gases (10 to 1000 sccm); Published comparative evaluation of thermal mass flow controllers.

FY 1996 Developed model for residual gas analyzers that qualitatively describes commercial RGA performance in high pressure operation (0.001 to 0.1 Pa); Developed primary and transfer flow standards for inert gases (0.1 to 10 sccm); Conducted initial on-site flow proficiency tests with four mass flow controllers manufacturers (5 to 1000 sccm).

FY 1997 Develop a methodology to optimize commercial RGAs for semiconductor process control; Perform flow proficiency tests with gas handling suppliers to the semiconductor industry; Develop primary flow standards with uncertainties less than 0.05% (1 to 1000 sccm).

FY 1998 Develop and test techniques for in-situ validation of residual gas analyzers used semiconductor process control; Develop stable portable flow standards which are compatible with corrosive and/or toxic gases used in semiconductor processes.

5. Moisture Concentration Measurements in Process Gases

FY 1994 Completed design for low frost-point, precision moisture generator with operating range from 1-5 ppb to 1000 ppm.

FY 1995 Demonstrated quantitative capability of optical cavity ring-down spectroscopy (CRDS) for trace contaminant measurement; Completed construction of prototype low frost-point moisture generator.

FY 1996 Complete round robin in cooperation with SEMI, evaluation low moisture concentration measurement instruments and transfer standards in the 1 to 100 parts per million range; Demonstrate quantitative measurement of contaminants in gases below 1 ppm using cavity ring-down spectroscopy.

FY 1997 In cooperation with SEMI, evaluate performance of permeation tube working standards for moisture concentrations in the 10 - 100 parts-per-billion range; Demonstrate CRDS-based detection of water vapor at 1.39 micrometer using a pulsed laser source; Investigate diode-laser-based CRDS at 1.39 micrometer.

6. Metrology for Contamination-Free Manufacturing

FY 1995 Fabricated particulate samples used to establish detection limits for commercial tools; Completed design of rotating-disk chemical vapor deposition (CVD) reactor.

FY 1996 Completed fabrication of the reference rotating disk CVD reactor which will be used to validate nucleation and growth models for contaminant particles.

FY 1997 Begin in-situ measurements in reference CVD reactor to map regimes under which particle formation occurs during thin film growth and the effect of particles on film morphology; Commission 300 mm wafer-capable plasma reference reactor.

7. Thin Film Profile Measurement Methods and Reference Materials

FY 1995 Introduced SRM 2137 as first boron implant in silicon standard; Organized profilometry round-robin for Secondary Ion Mass Spectrometry (SIMS) crater depth measurements.

FY 1996 Developed neutron activation analysis protocol for arsenic in silicon; Began developing methods for ultra-shallow profiling using SIMS.

FY 1997	Complete certification and issue arsenic implant standard; Use SIMS rotating sample stage to demonstrate depth resolution improvement.
FY 1998	Issue SIMS depth resolution reference material; Investigate SIMS molecular ion beam source for ultra-shallow profiling.

8. Radiometric Metrology for Deep Ultraviolet Lithography

FY 1995	Developed method for calibrating discharge lamps used for ultraviolet photoresist stabilization; Continued work with commercial partner to improve accuracy of ultraviolet probes.
FY 1996	Upgraded refractometer to enable high-accuracy refractive-index measurements and began measurements for SEMATECH/Lincoln Labs near 193 nm; Began development of dielectric barrier discharge source as potential ultraviolet/deep ultraviolet standard.
FY 1997	Perform high-accuracy measurements of the refractive index of optical materials and their temperature coefficients near 193 nm for SEMATECH/Lincoln Labs; Build new refractive-index-measurement apparatus based on interferometry, capable of improved accuracy.
FY 1998	Make refractive-index measurements of deep-ultraviolet materials at 193 nm, 157 nm, and shorter wavelengths as needed for the design of next-generation semiconductor photolithography steppers.

9. Wafer and Chuck Flatness

FY 1995	Interferometric flatness metrology system for 300 mm wafers demonstrated; Thickness variation interferometer conceived and demonstrated as lab breadboard; Rapidly renewable lap conceived and demonstrated at 150 mm.
FY 1996	Completed 300 mm flatness interferometer and made initial chuck distortion measurements; Initiated commercialization activities on thickness interferometer; Scaled up lap to 300 mm, demonstrated rapid silicon polishing process and potential for chem-mechanical process (CMP) applications.
FY 1997	Commercialize renewable lap and develop CMP applications; Install hardened thickness interferometer and complete commercialization; Demonstrate combined thickness and flatness metrology to separate thickness variation effects from distortion at 300 mm aperture.

10. Optical Scattering for Wafer Surface Metrology

FY 1995	Developed a new standard reference material for low-level bidirectional reflection distribution function (BRDF) measurements; Verified accuracy of new low-level BRDF instrumentation to better than 1%.
FY 1996	With a commercial partner, developed reference wafers to calibrate fab line haze meters; Developed methodology for characterizing microroughness-induced optical scatter instrumentation.
FY 1997	Investigate scattering from particles on silicon surfaces to determine size and composition; Characterize polarization of light scattered from different scattering sources on silicon wafers; Develop software to allow manufacturers of commercial wafer inspection systems to report the response functions of their instruments.
FY 1998	Investigate scattering from particles on patterned silicon surfaces; Investigate scattering from crystal-originated particles.

11. Improved Characterization of Microroughness and Near-Surface Defects

FY 1995	Developed advanced scanning scattering microscope using latest optical techniques; Developed positioning system for the NIST small artifact instrument.
FY 1996	Began measurements of interface topography of buried silicon dioxide/silicon interfaces.
FY 1997	Complete study of silicon dioxide/silicon interface topography using the scanning scattering microscope; Collaborate with MIT Lincoln Labs to solve problems of thin silicide characterization.
FY 1998	Use grazing incidence x-ray photoelectron spectroscopy to analyze chemical structure of ultrathin dielectrics on silicon; Develop ultrahigh resolution transmission electron microscope cross-sectional chemical analysis capability.

12. High Accuracy Two Dimensional Measurements

FY 1995	Developed and tested control system for M48 coordinate measuring machine; Began characterization of system accuracy for measurement of large (up to 750 mm x 750 mm) grid plates; Developed and tested positioning system for small grid measuring machine (M4).
FY 1996	Made first commercial calibrations of large grid plates on M48 coordinate measuring machine; Typical accuracy for 500 mm x 500 mm grid is 0.40 micrometer; Completed development of small 200 mm x 200 mm measuring machine (M4); Began characterization of geometric errors and development of error map; Developed robust edge-finding algorithms for system, and began study of methods divergence problems for grid mark edge finding.
FY 1997	Finish characterization of M48, including comparisons of one-dimension measurements with the NIST Line Scale Interferometer; Begin joint project with Nano-scale Metrology Group to develop similar instruments; Begin design of industry interlaboratory tests of length measurement capabilities; Continue study of calibration algorithms for grid calibration; Includes partial closure calibration of grid and machine geometry by multiple in multiple positions and orientations.
FY 1998	Participate in interlaboratory tests of measurement accuracy for grid plates; Continue study of edge finding methods; develop methods to reduce these effects between industrial measuring systems; Develop robust measurement algorithms to measure grids that provide control data for SPC.

13. Improved High Temperature Thermometry

FY 1995	Completed selection and stability testing of platinum/palladium (Pt/Pd) thermocouples from 0 °C through 1300 °C**.**
FY 1996	Completed reference function data collection for Pt/Pd thermocouples at NIST and the Italian national standards laboratory, Instituto di metrologia "G. Colonnetti" to 1500 °C; Developed a system for calibration of thin film thermocouples on silicon wafers up to 900 °C; Selected materials system, including thermocouples, insulators, and bond coats for use on silicon wafers.
FY 1997	Derive and publish reference function for Pt/Pd TCs from 0 ˚C to 1500 ˚C. The Pt/Pd thin-film thermocouple system on 200 mm diameter silicon wafers will be developed to have superior accuracy to any commercial system. Such

a system will be used to calibrate radiation pyrometers for rapid thermal processing systems.

FY 1998 The design and fabrication of thin-film thermocouples and the methodology of their use in calibrating radiation pyrometers up to 900 ˚C for rapid thermal processing use will be specified and made available for commercialization; A new materials system for a thin-film thermocouple designed for operation up to 1100˚C will be developed.

14. Micromechanical Measurements

FY 1995 Measured local strains around a via in a multichip module-laminate (MCM-L) high density interconnect structure; Improved microtensile machine with installation of piezoelectric drive and controller.

FY 1996 Tested polysilicon in sample microelectromechanical systems (MEMS) devices; Extended electron beam moiré measurements to biaxial displacements; Applied technique to measurement of thermal deformation of conductive adhesives.

FY 1997 Measure thermomechanical deformations in low-dielectric-constant, back-of-the-chip interconnect structures; Measure local stresses and strains in VLSI interconnects; Measure mechanical properties of metals for low-cost solder bumps.

FY 1998 Measure local crystallography, stresses, and strains in stress-voided multilevel interconnect structures; Measure thermal conductivity in thin films from industry using microscale test structures; Use e-beam moiré to evaluate effects of thermal cycling on interconnect structures.

15. Solderability Measurements and Optimization

FY 1995 Results of NIST solderability research included in the Institute for Interconnecting and Packaging Electronic Circuits (IPC) Joint Industry Standard.

FY 1996 Research showing errors present in the interpretation of dynamic and nonisothermal wetting balance tests published in ASME Journal of Electronic Packaging.

FY 1997 Determine effect of oxide and flux thickness on solder meniscus shape; Relate to errors present in wetting balance test for solderability.

FY 1998 Develop theory for reactive wetting; Apply theory to design of improved wetting test.

16. Thermoset Cure and Performance

FY 1995 Showed that moisture accumulates as liquid-like water at polymer/silica interfaces; Demonstrated new method for determining thermal diffusivity of thin polymer films on silicon.

FY 1996 Demonstrated capacitance cell measurement method for out-of-plane coefficient of thermal expansion of polymer thin films. Using near infrared spectroscopy, concluded that moisture absorbed from a humid environment by unfilled polyimide and epoxy molding resin is molecularly dispersed.

FY 1997 Provide data on hygroscopic out-of-plane expansion of thin polymer films used in electronic packaging; Work with standards-setting bodies to consider adopting capacitance cell technique for measuring expansion of thin films.

FY 1998	Develop measurement technique for surface in-plane thermal and hygroscopic expansions of thin polymer films confined to a non-expanding substrate; Develop and validate code for predicting expansion of thin polymer films confined by a substrate.

17. Thin-Film Reference Materials

FY 1995	Project was under development.
FY 1996	Provided titanium nitrate (100 nm) films accurately characterized for thickness, contamination, stoichiometry, density, and roughness to SEMATECH companies through the Analytical Laboratory Managers Working Group; Characterized epi-silicon on silicon wafers for a major microprocessor manufacturer; Improved production and characterization capabilities for layered structures in general.
FY 1997	Begin validation tests of available modeling software including non-specular scattering; Characterize platinum reference thin films for a major semiconductor manufacturer; Determine the role of added hydrogen in altering growth of ion-beam sputtered films; Implement vacuum reflectometer for efficient silicon oxide film thickness measurement and expanded structural characterization.
FY 1998	Build dedicated reflectometer for clean characterization of layered structures on 200 mm wafers; Improve modeling of interlayer structures and apply to diffusion studies.

Metrology for Nanoelectronics

Project Leader: Joseph G. Pellegrino

Staff: 2.5 Professionals, 1.5 Technicians

Funding level: $0.8 M

Funding sources: NIST (100%)

Objective: Provide technological leadership to semiconductor and equipment manufacturers by developing and evaluating the methods, tools, and artifacts needed to improve the state of the art in compound-semiconductor growth and nanometrology (measurements on a scale of 10 to 100 nanometers). Provide measurements of growth and structural parameters in addition to fabrication properties required for the reliable manufacture of nanostructure devices. Develop research materials and methods to improve measurement standards.

Background: The yield and reliability of nanostructure devices (having feature sizes between 10 and 100 nanometers) critically depend on the quality of the materials and processes that are used to manufacture them. Industry needs NIST to provide the methodology, both experimental and theoretical, to evaluate and improve these materials and processes at resolutions on the order of 10 nanometers. Improved materials growth, evaluation techniques, and models are needed by the compound-semiconductor industry to manufacture useful and reliable devices based on advanced quantum phenomena. There is a great need for standard reference artifacts to reduce measurement ambiguities and uncertainties.

Current Tasks:

1. Develop an in-situ metrology effort for the real-time, in-situ characterization of advanced III-V epilayers

FY 1994	Designed state-of-the-art molecular beam epitaxy (MBE) facility to specifically address real-time, in-situ measurement of growth parameters critical to improved performance of lattice-matched, thickness-dependent, compositionally controlled heterostructures. Designed a unique state-of-the-art X-ray detector in order to implement, for the first time, X-ray fluorescence as an in-situ compositional probe during MBE growth.
FY 1995	Designed equipment and software for in-situ optical reflectometry; Designed multiple-wavelength reflectometer to improve thickness resolution to 5 nanometer level.
FY 1996	Used in-situ X-ray fluorescence capability in MBE growth chamber to measure and control composition and possibly thickness of MBE layers; Equipped MBE with in-situ ellipsometer for measuring thickness,

composition, and roughness of MBE layers; Initiated plans to implement pyrometric interferometry as an in-situ optical probe to measure temperature.

FY 1997 Correlate various in-situ measurements of the alloy composition and thickness, compare with the results of ex-situ techniques, and address differences.

FY 1998 Develop an in-situ X-ray-based capability to determine epilayer thickness and measure strain in real time during growth; Develop research materials and methods to improve standards.

2. Develop a measurement infrastructure pertinent to the interface characterization of advanced III-V heterostructures

FY 1993 Characterized interface roughness in low-order aluminum arsenide/gallium arsenide superlattices and determined the influence of the gallium arsenide buffer layer thickness on the subsequent superlattice interface quality; Obtained smoother interfaces in samples with buffer layers with a thickness 250 nanometers and greater; Using high-resolution X-ray diffraction, showed that the quality of the superlattice interfaces is markedly affected by the growth technique; Also found interfaces were sharper in a migration-enhanced epitaxy sample than in an equivalent superlattice sample grown by the interrupted-growth technique.

FY 1994 Measured anisotropic strain and tilt along orthogonal directions in indium aluminum arsenide/indium phosphide heterostructures used in optoelectronic devices; Used the X-ray standing-wave technique to learn that the buried indium arsenide strained layer in Pseudomorphic High Electron Mobility Transistors (PHEMTs) is only 76% coherent. (Collaboration with Materials Science and Engineering Laboratory)

FY 1995 Correlated roughness properties of MBE-grown aluminum arsenide/gallium arsenide superlattices with carrier mobility in the associated modulation-doped field-effect transistor (MODFET) channel layers; Demonstrated that interface roughness is a function of the growth temperature and that room temperature X-ray diffraction spectra of the roughness can be related to the measured electron mobility in the channel.

FY 1996 Studied interface and structural properties with X-ray diffraction and X-ray standing-wave techniques to optimize layer quality. (Collaboration with Materials Science and Engineering Laboratory)

FY 1997 Develop measurement capability to assess the effects of interfaces on the device performance of dual-pulsed pseudomorphic high electron mobility structures (PHEMTs).

FY 1998 Measure the influence of the interface quality on the performance of non-(100) oriented advanced heterostructures used in both electronic and optoelectronic applications.

3. Develop and address measurement issues pertaining to nanostructure characterization and fabrication

FY 1991 Generated nanometer-scale patterns on hydrogen-passivated Si by using scanning tunneling microscope (STM) techniques; STM-patterned oxide serves as a mask for selective-area GaAs heteroepitaxy on silicon, an essential step in mating GaAs and silicon device technologies. (Collaboration with Manufacturing Engineering Laboratory)

FY 1992	Grew high-quality GaAs samples for the quantum-Hall resistance standard. (Collaboration with Electricity Division)
FY 1993	Studied nanometer-scale oxides patterned by means of scanning tunneling microscopy and showed they are readily generated in an air ambient, easily imaged by scanning electron microscopy and other microprobe techniques, capable of surviving realistic processing environments, and useful as masks for etching and selective area growths. (Collaboration with MEL)
FY 1994	Designed a new series of superlattice structures to increase the confinement of the optically produced carriers and obtain stronger exciton peaks. (Collaboration with the University of Iowa)
FY 1995	Continued scanning tunneling microscopy effort (Collaboration with MEL); and made contributions to single electron transistor effort (Collaboration with Division 811). Fabricated “shadow masks” in MBE for use in growing vertically interdigitated optical switches. The interdigitated sample has been metallized and shows proper diode behavior. Characterized sample by photoreflectance while optically biased. Data indicate an upshift of the quantum well energy, as predicted. (Collaboration with the University of Iowa)
FY 1996	Installed focused-ion-beam (FIB) lithography system in MBE chamber for patterning III-V and possibly silicon wafers; Assisted optimization of STM system for measuring nanostructures; Grew specialized heterostructures for electronic and optoelectronic devices. (Collaboration with University of Iowa and others)
FY 1997	Fabricate quantum wires and dots on wafers with FIB. Perform MBE regrowth on pre-FIB processed substrates to investigate feasibility of three-dimensional device stacking. Utilize FIB lithography to develop research artifacts for improved standards.
FY 1998	Utilize FIB lithography to develop research artifacts for improved standards.

Optical Characterization Metrology

Project Leader: Paul M. Amirtharaj

Staff: 3.0 Professionals, 1.0 Post Doc

Funding level: $0.9 M

Funding sources: NIST (90%), Other Government Agencies (10%)

Objective: Develop and implement advanced and robust optical probes needed by the semiconductor industry. Develop optical probes for the analyses of silicon-related materials behavior including ultrathin insulator layers on silicon IC wafers. Advance and optimize modulation and selective excitation spectroscopies for the study of technologically important semiconductor materials and microstructures. Develop standard research materials and methods and compile data to improve standards.

Background: Manufacturers of electronic components for a wide variety of applications, extending from digital circuitry for computers to light emitters for optical communication, need reliable analytical methods and well-established standards for characterizing the behavior of elemental and compound semiconductor materials. The continual reduction in feature size set forth in the National Technology Roadmap for Semiconductors for increased packing density and the complex optoelectronic device structures that use 10 to 100 layers place stringent demands on the current analytical probes. Further device advances can be commercially realized only with the enhanced yield possible with sophisticated and dependable characterization. Optical and electrical activity form the foundation of all the major electronic devices today. Optical probes are attractive and powerful because they are contactless and nondestructive, compatible with any transparent gas, capable of remote sensing, and compatible with hostile environments. Optical probes are useful for in-situ probing during materials growth, on-line processing diagnostics, and preprocessing screening and hence can greatly aid in the efficient and economic manufacture of electronic devices.

Current Tasks:

1. Develop metrology to identify and quantify impurities in silicon

   FY 1988 Assisted American Society for Testing and Materials (ASTM), a voluntary standards organization in the U.S., though its Subcommittee F1.06 in a pilot study on the determination of trace impurities in silicon by photoluminescence; Determined the conversion coefficient for infrared measurement of oxygen in silicon. Wrote two new standard test methods adopted by ASTM: Method F 1188, Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption, and Method F 1189, Using Computer-Assisted Infrared Spectrophotometry to Measure the Interstitial Oxygen Content of Silicon Slices Polished on Both Sides.

FY 1989	Published archival summary and extended report of analysis of International Round-Robin-on-Oxygen conversion-factor for infrared measurements.
FY 1990	Developed fully automated analytical procedure to study oxygen in double-side-polished silicon wafers.
FY 1991	Completed installation and testing of high resolution and high-stability Fourier transform interferometers for impurity analysis in silicon.
FY 1992	Completed oxygen-in-silicon Standard Reference Material (SRM) production methodology.
FY 1993	Completed certification and related measurements for 100 sets of SRM 2551 for Interstitial Oxygen in Silicon. Analysis of data indicates an uncertainty of certification, relative to the master calibration set, of better than 0.17% (2σ). SRMs are required by integrated circuit manufacturers to determine oxygen concentrations.
FY 1994	Demonstrated the use of Fourier transform infrared (FTIR) absorption for measurement of boron and phosphorous in high-purity silicon at densities of less than 10^{12} per cubic centimeter.
FY 1995	Applied the above capability for Defense Production Act-Title III high-purity silicon materials qualifications. NIST was requested to provide this assay of dopants by the Department of Defense.
FY 1996	Applied spectroscopic and photoconductive probes to investigate the origin of persistent-photoconductivity and/or slow traps in integrated circuit grade silicon. Deep traps with activation energies >0.3 electron-volts and delay time of >100 seconds observed in B-doped Czochralski-silicon. (Collaboration with the Electrical Characterization Project)
FY 1997	Develop FTIR methodology to produce oxygen-in-silicon SRM, with concentration in the 10 to 13 parts-per-million range, to respond to recent requirements of the silicon integrated circuit industry.
FY 1998	Develop FTIR methodology to investigate electrically active impurity complexes including oxygen-related thermal donors.

2. Develop and apply nondestructive optical probes of the electronic behavior of technologically important semiconductor materials and device structures

FY 1990	Developed and published “A Software Program for Aiding the Analysis of Ellipsometric Measurements, Simple Spectroscopic Models” as NIST Special Publication 400-84.
FY 1991	Completed building and testing a state-of-the-art spectroscopic ellipsometer with near monolayer sensitivity; Applied instrument to study real-time oxidation of the gallium arsenide surface.
FY 1992	Provided optical characterization of silicon carbide for X-ray mask application and cadmium zinc telluride substrates for infrared materials growth.
FY 1993	Achieved a critical advance in the quantitative understanding of the optical properties of the silicon dioxide/silicon interface region by conducting accurate spectroscopic-ellipsometry measurements and by developing an analysis that, for the first time, comprehensively accounted for strain and microroughness. This was a necessary step in the development of thin ($d < 10$ nm) silicon dioxide/silicon SRMs.
FY 1994	Advanced the state of the art of photoreflectance spectroscopy for semiconductor analyses through the use of double-modulation and multiple-pump beams. Detailed analysis of complex laser structures was now possible.

FY 1995	Completed one-of-a-kind selective-excitation system operable in the 350 to 1100 nanometer range and initiated comprehensive defect and impurity analyses in gallium nitride.
FY 1996	Completed automation of the selective excitation system, with capability from the ultraviolet to the infrared region of the optical spectrum, for high-resolution optical spectroscopy. Discovered several previously unreported impurity and defect features using system to investigate gallium nitride and related materials.
FY 1997	Conduct selective-excitation spectroscopy and analysis of technologically important compound semiconductor materials and microstructures; Develop optical probes capable of detecting ultrathin SiO_2 layers on silicon and analyzing their properties.
FY 1998	Extend above capability to study spatial (lateral) variations in multilayer wafers.

3. Provide coordination and leadership to industry in optical characterization and related activity

FY 1989	Organized and hosted the International Conference on Narrow-Gap Semiconductors and Related Materials in Gaithersburg, MD, June 1989.
FY 1990	Edited and published Proceedings of the International Conference on Narrow Gap Semiconductors.
FY 1991	Developed detailed questionnaire on optical characterization techniques needed by the industry; Presented invited tutorial talk, "Optical Characterization of Electronic Materials," at two-day symposium, Microanalysis of Electronics, organized by ASM International and NIST Office of Microelectronics Programs.
FY 1992	Distributed to major semiconductor companies a questionnaire regarding the use of optical characterization techniques for materials and device analysis by the semiconductor industry.
FY 1993	Wrote chapter on "Optical Properties of Semiconductors" for the *Handbook of Optics*, second edition, for the Optical Society of America and McGraw Hill; Provided review of all important optical properties and techniques for measuring them; Second mailing of optical characterization survey sent out.
FY 1994	Presented an invited review entitled "Optical Properties and Characterization Methods for HgCdTe" at the 1993 U.S. HgCdTe Workshop that emphasized industrial applications for semiconductors. Mercury cadmium telluride (HgCdTe) is a material used to make detectors for infrared light. Carried out analysis of optical characterization survey results.
FY 1995	Organized and conducted the International Workshop on Semiconductor Characterization with 280 attendees, 40 invited speakers and 80 poster papers. Workshop provided up-to-date reviews of major characterization issues; Organized and conducted the Workshop on Planning for Compound Semiconductor Technology, attended by 60 participants and 6 invited speakers, with a panel discussion. Participants agreed on consensus-based planning to help the North American segment remain competitive.
FY 1996	Presented invited paper entitled "Double Modulation Photoreflectance" at the Symposium on Diagnostic Techniques for Semiconductor Materials Processing, Materials Research Society Fall Meeting, November 1995; Published Proceedings of the International Workshop on Semiconductor Characterization by the American Institute of Physics Press; Published and

distributed to industry NIST Special Publication 400-98 containing results of the Optical Characterization Survey.

FY 1997 Contribute chapter on optical properties to book on properties of narrow-gap II-VI semiconductors to be published by Chapman-Hall, United Kingdom; Edit proceedings of the 1996 U.S. Workshop on the Physics and Chemistry of II-VI Materials.

4. Compile near-edge fundamental parameters for III-V binary semiconductors

FY 1996 Initiated the Standard Reference Data (SRD) Project entitled, "Near Band-Edge Fundamental Parameters for III-V Binary Semiconductors" and reviewed relevant published literature.

FY 1997 Complete above project for technologically important binary materials.

FY 1998 Compile changes in above parameters in doped materials as a function of carrier density.

FY 1999 Compile above parameters for selected ternary alloys.

Scanning-Probe Microscope Metrology

(New name for Electrical Characterization Metrology)

Project Leader: Joseph J. Kopanski

Staff: 4.0 Professionals

Funding level: $0.8 M

Funding sources: NIST and OMP (90%), Other Government Agencies (10%)

Objective: Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply scanning-probe microscopes and other electrical characterization to semiconductor materials and processes; provide silicon and compound-semiconductor manufacturers with advanced scanning-probe electrical metrology techniques and models to improve device performance and reliability.

Background: The reduction in feature sizes to near 100 nanometers predicted by the goals of the semiconductor industry for the early 21st century requires new and improved measurement methods to characterize materials and processes to the required 10 nanometer resolution scale. Industry needs NIST to provide the methodology, both experimental and theoretical, to evaluate and improve materials and processes by implementing scanning-probe microscope-based and traditional electrical techniques. Measurements of the dopant density, lifetime, and mobility of charge carriers in wafers and thin layers are essential for materials and process qualification. The National Technology Roadmap for Semiconductors has challenged NIST with responsibility for developing the technology needed to determine the dopant distribution across a processed silicon wafer to a resolution of 20 nanometers. Scanning capacitance microscopy is being developed as a new tool to achieve this goal.

Current Tasks:

1. Develop scanning-probe microscopy and models for dopant profiling and overlay

FY 1989	Demonstrated two-dimensional mapping of silicon resistivity striations with resolution of 40 micrometers by high-density four-probe structures.
FY 1990	Demonstrated and verified high-spatial-resolution resistivity mapping with ion-implanted test structures and theoretical modeling; Showed that lateral resistivity variations over dimensions as small as 45 micrometers can be mapped, which has important application to gallium arsenide and mercury cadmium telluride materials.
FY 1991	Applied fine-scale resistivity mapping technique to specimens of mercury cadmium telluride; Showed that nonuniformity patterns are correlated with the type of crystal growth, LPE (liquid-phase epitaxy) or SSR (solid-state recrystallization).

FY 1992 Prepared detailed specifications for a scanning tunneling/atomic force microscope for scanning capacitance microscopy (SCM); the microscope is one of the first to be made with a large sample stage, compatible with semiconductor wafers with diameters to 250 millimeters. Began development of the capacitance-sensitive circuit and theoretical modeling of the SCM measurement.

FY 1993 Designed, constructed, and tested an SCM for nanoscale (10 to 100 nanometers) profiling of semiconductor junctions; the design is the first to take advantage of incorporating a commercial atomic force microscope (AFM).

FY 1994 Obtained capacitance-voltage curves with the SCM as a function of probe position. Implemented tapping-mode capability on SCM to reduce damage to probe and specimen and give improved reproducibility and signal-to-noise ratio. Developed three-dimensional collocation code to solve Poisson's equation for SCM.

FY 1995 Demonstrated a new mode of scanning capacitance microscopy: imaging the high-frequency capacitance directly. This enables imaging of metal lines on an insulating substrate for overlay metrology. Produced two-dimensional (2D) images of dopant profiles from cross-sectioned silicon wafers with better than 30 nanometer resolution; Modeled the probe-ambient-insulator region with commercial code, which solves Laplace's equation in three dimensions (3D); Combined solutions with those from 3D collocation code for semiconductor region to obtain total solution of electric potential; Computed capacitance as a function of bias voltage for uniformly doped silicon wafer.

FY 1996 Established reliable techniques to obtain SCM data of carrier profiles; Applied SCM method to overlay metrology; Obtained solutions in 2D and 3D for the charge density in doped silicon wafers and simulate SCM data; Developed useful, simple methodology to relate SCM data to dopant profiles.

FY 1997 Interact strongly with equipment and user community to transfer NIST technology; Validate SCM model and methodology from measurements on well-known samples provided by industry; Use developed code to produce model database; investigate ways of including dopant gradient effect; Implement data conversion methodology in a user-friendly and 2D format; Develop tapping mode SCM for overlay measurements; Identify SRMs needed to support industry use of SCM measurement standards.

FY 1998 Improve spatial resolution and accuracy of SCM 2D dopant profile measurement; Initiate investigation of the effects of illumination on scanning probe-microscopy measurements.

2. Perform bulk/thin film magnetotransport analyses of carrier densities and mobilities; develop silicon resistivity Standard Reference Materials (SRMs)

FY 1989 Completed extensive evaluation of a technique for impedance measurement using time varying signals for high-resistivity silicon (from 2 to 50 ohm centimeter); Developed silicon resistivity SRMs.

FY 1990 Demonstrated validity of the impedance technique for measuring high-resistivity silicon by comparison with traditional techniques; Certified 155 sets of bulk silicon resistivity SRMs (51 mm diameter, 0.01 to 180 ohm centimeter); Transferred, to SRM office, 101 sets of these and the final 40 sets of spreading resistance SRMs.

FY 1991	Certified over 400 50.8 millimeter (2 in.) diameter wafers having resistivities, from 0.01 ohm centimeter to 200 ohm centimeter, for use in multiwafer silicon resistivity SRM sets; Established facility for variable magnetic field transport measurements over the temperature range from 10 to 400 kelvin and tested specimens of aluminum gallium arsenide/gallium arsenide, indium antimonide/indium arsenide, and mercury cadmium telluride; Developed a procedure for efficient identification of single- or multiple-carrier conduction.
FY 1992	Developed and applied a general technique for analyzing multicarrier conduction; Made extensive Hall and resistivity measurements on several structures; Continued work on silicon SRMs.
FY 1993	Developed a simple, accurate measurement method for determining the electron density and Hall mobility of semiconductor layers, based on the magnetic-field dependence of the two-terminal magnetoresistance of a rectangular layer; Applied this method to characterize accumulation layers of n-type mercury cadmium telluride infrared (IR) detectors; Provided NOAA with characterization study of mercury cadmium telluride detectors used in Geostationary Operational Environmental Satellite weather satellites; Completed certification and system control measurements for 135 units of SRM 2547 100 millimeter diameter silicon resistivity at the 200 ohm centimeter level.
FY 1994	Established high-field magnet facility; Studied two-dimensional magnetophonon effect and universal conductance fluctuations in gallium arsenide/aluminum gallium arsenide heterostructures grown in Division's MBE system as well as in silicon/germanium heterostructures grown at the Naval Research Laboratory; Continued certification of silicon SRMs.
FY 1995	Determined carrier densities and mobilities in mercury cadmium telluride, III-V, and high-resistivity silicon samples; Completed calculations of mobility of gallium arsenide, including electron-electron and electron-phonon scattering; Continued to measure 100 millimeter silicon resistivity SRMs; Discovered photosensitivity of resistivity to fluorescent room light, which requires that two of the seven SRMs (1 and 10 ohm centimeter) be removed from series; Showed need for further research of cause of effect before proceeding with these two SRMs.
FY 1996	Provided information from electrical methods as to the cause of photoresponse in several of the 100 millimeter diameter silicon resistivity SRMs; Characterized the electrical properties of samples grown in molecular beam epitaxy machine, fabricated in focused ion beam machine, or supplied by industry.
FY 1997	Deliver 100 mm resistivity SRMs for sale to industry; Characterize traps responsible for photoeffect in SRM p-type silicon by deep level transient spectroscopy and photoconductivity; Develop instrumentation and theoretical understanding to implement the photo-Hall effect and magnetoresistance measurements.
FY 1998	Apply developed electrical characterization techniques to advanced materials fabricated by the Group and others; Assess needs for further SRMs and measurement standards.

3. Develop and apply models of scanning electron microscope signals for critical-dimension metrology (Collaboration with Manufacturing Engineering Laboratory)

FY 1993	Surveyed and used existing code for modeling scanning electron microscope (SEM) signals.
FY 1994	Wrote and documented a new Monte Carlo code, MONSEL-I, to simulate the transmitted and backscattered signals from a multilayer specimen in an SEM; Code has been used to provide a quantitative description of the signals from a gold line on a silicon substrate used in critical-dimension metrology.
FY 1995	Completed improved Monte Carlo code, MONSEL-II, for simulating transmitted, backscattered, and secondary electron signals in SEM; Model target is three parallel lines on multi-layer substrates; Completed work on MONSEL-III, a code for simulating short lines and vias as well as tilted substrates; Compared results of simulations with those from measured scans to obtain line edge locations to less than 10 nanometers.
FY 1996	Developed methodology to optimize Monte Carlo simulations of SEM signals and enhance codes as required.
FY 1997	Advise industrial users of MONSEL-II and MONSEL-III regarding their proper use, and extend codes based on feedback from user community; Provide modeling for development of SRMs for critical-dimension metrology; Task completed; Related work continues in the Manufacturing Engineering Laboratory.

Thin-Film Process Metrology

Project Leader: James R. Ehrstein

Staff: 3.2 Professionals, 2.0 Technicians, 1.0 Contractor

Funding level: $0.8 M

Funding sources: NIST and OMP (100%)

Objective: Develop new and improved measurements, models, data and reference materials to enable better and more accurate measurements of select critical silicon-technology thin-film process parameters.

Background: Fabrication of thin films of various types is a fundamental building block in semiconductor device fabrication. The rapid, continuing requirements for ever thinner films places increasingly stringent requirements on the composition and structure of those films. This, in turn, places increasingly stringent requirements on the metrology tools and procedures used for process development and process monitoring. The drive in the industry is toward establishing in-situ process-monitoring capabilities for all major process steps. Yet as layers and structures are refined and shrunk, improved in-line, at-line, and off-line capabilities will also be necessary to verify the relations between material parameters resulting from the process steps and the parameters being monitored in situ. Among the thin-film process metrology challenges, two are targeted initially: dielectric layers, particularly gate dielectrics, and ion-implant dosimetry. The National Technology Roadmap for Semiconductors identifies robust gate dielectrics with 5 nanometer thickness as a specific on-chip materials issue that will impact the ability to achieve the 15-year goals of the Roadmap. NIST work will provide the metrology support required for the controlled processing of these films in the semiconductor manufacturing environment. The need for implanted reference materials for process transfer and industry reference is cited in “Metrology Roadmap: A Supplement to the National Technology Roadmap for Semiconductors.”

Current Tasks:

I. Establish and transfer basis for accuracy of measurement of silicon-related dielectric layers, in both at-line and in-situ modes.

1. Establish traceability to NIST for measurements of critical dielectric layers of silicon

FY 1988	Certified and released the first Standard Reference Materials (SRMs) for thickness of silicon dioxide, at thicknesses from 50 to 200 nanometers.
FY 1989	Developed computer code and released documentation for ellipsometric analysis of thickness of dielectric layers and interface region.
FY 1992	Developed and certified 14 nanometer and 25 nanometer silicon dioxide thickness SRMs.

FY 1994	Developed and certified 10 nanometer silicon dioxide thickness SRMs; Completed intercomparison with nine select laboratories for measurements of 10 nanometer oxides; Demonstrated interlaboratory repeatability consistent with industrial requirements. National Technology Roadmap for Semiconductors reaffirms critical nature of ultrathin gate oxide fabrication control.
FY 1995	Developed cooperative program with commercial source of reference materials to establish traceability to NIST for thin oxide materials.
FY 1996	Initiated CRADA experiments to establish traceability to NIST of ellipsometer-based Reference Materials.
FY 1997	Plan and conduct workshop for key industry members interested in standards and traceability to develop guidance for NIST in dielectric standards issues.
FY 1998	Implement recommendation for improving traceability.

2. Develop understanding of relation between silicon/dielectric layer interface roughness and optical characterization techniques for dielectric layer thickness and index

FY 1994	Used spectral ellipsometry measurements to validate interface model used for single-wavelength oxide Reference Material certification; The National Technology Roadmap for Semiconductors affirms need to understand and control surface on which gate oxide is grown.
FY 1995	Established capability for "Weak Localization" measurement technique to extract quantitative measure of electronic roughness at a layer-interface.
FY 1996	Extended this technique to the quantitative measurement of interface roughness in typical silicon metal oxide-semiconductor field-effect transistor (MOSFET) test structures.
FY 1997	Compare experimentally electrical measurements of dielectric and interface properties with optical, or other "beam-probe" determinations of those properties.
FY 1998	Begin to improve physical models for the interpretation of electrical and optical data.

3. Develop high-accuracy database for optical constants of silicon and its dielectric layers at elevated temperatures used for integrated circuit processing

FY 1995	Contracted for design and fabrication of customized vacuum chamber with in-situ ellipsometry and high-temperature film growth capability; The National Technology Roadmap for Semiconductors asserts need for in-situ metrology of film thickness and gate dielectric composition.
FY 1996	Installed test chamber at NIST; Began test and evaluation of chamber.
FY 1997	Complete test of chamber and instrumentation, development of control and analysis software; Measure optical constants for silicon substrates at temperatures to 1000 °C.
FY 1998	Begin program of determining optical constants of critical thin films of silicon at elevated temperatures.

II. Develop reference materials for ion implant dosimetry

FY 1992	Established need and potential guidelines at SEMATECH-sponsored workshop for transfer standards between implant dose and sheet resistance.
FY 1995	Initiated program to develop reference materials for ion implant dosimetry; Provided leadership and planning input to Third International Workshop on the Measurement and Characterization of Ultra-Shallow Doping Profiles in Semiconductors; Edited Workshop Proceedings.
FY 1996	Modeled the sensitivity of the implant dose/sheet resistance relation (for boron) to starting material and implant condition parameters.
FY 1997	Complete implant cycle sensitivity determinations; Determine optimum process cycle; Determine whether dose standard can be done directly with a specific boron isotope; Begin certification process for implant dose transfer standard, and whether dose/sheet resistance standard can be implemented at target level of 1% uncertainty.
FY 1998	Initiate fabrication and certification of implant dose/sheet if stability and process cycle tests indicate that target uncertainty is likely to be met.

Metrology for Simulation and Computer-Aided Design

(New project for FY 1997--see old project sheet "Metrology for Devices and Packages" for earlier related work.)

Project Leader: Allen R. Hefner

Staff: 4.5 Professionals, 1.0 Graduate Research Fellow, 0.1 Guest Researcher

Funding level: $1.1 M

Funding sources: NIST and OMP (93%), Other Government Agencies (7%)

Objective: Facilitate the efficient and reliable application of semiconductor computer-aided design (CAD) tools by: developing metrology necessary for providing model data, developing methods for simulator model validation, and providing simulation capability benchmarks; develop additional models and techniques necessary for advanced device, process, package, and system simulation; and support and participate in national and international standards and industry organizations.

Background: The project addresses needs at the boundary between model and simulator development and the application of computer-aided-design tools. The National Technology Roadmap for Semiconductor identifies modeling and simulation as cross-cutting technologies, and the availability of calibrated and easy-to-use technology computer-aided-design tools for device, process, and circuit simulation as areas requiring development and support to achieve the 15-year goals of the Roadmap. The Roadmap also states that using accurate computer models shortens time scales, lowers costs, and increases quality of each technology area. Advanced device electrical and thermal characterization procedures and validation of models used in computer-aided-design tools have not kept pace with the application of the new device types and processes. This project's goals are to develop methods and procedures and to support an industry infrastructure for establishing model accuracies.

Current Tasks:

1. Develop metrology for package thermal simulations, including environment

   FY 1997 Develop validation procedure for compact package models for use in computational fluid dynamics simulations in natural convection environment; Provide demonstration for multiple-package, highly confined, highly interacting system.

2. Develop metrology for integrated system simulation capability

   FY 1997 Develop required electrical measurement techniques to support integrated system simulation capability for U.S. Navy's Power Electronic Building Block Program's modules and chips and also the Partnership for a New

Generation Vehicle electric vehicle propulsion systems; Develop module thermal model for inclusion in system simulation programs.

FY 1998 Develop metrology for integrated package and circuit board electrical interconnect simulation and validation.

3. Develop models and validation metrology for circuit simulation

FY 1997 Begin draft of IEEE-recommended practices standards for Insulated Gate Bipolar Transistor (IGBT) model validation and microelectronic MOSFET model validation procedures. Apply model validation procedures to IGBT component libraries recently introduced in Pspice and Saber, and improve NIST IGBT model as appropriate. Investigate tools for improving analog-hardware-description language model development productivity.

4. Develop physics, validation metrology, and benchmarks for device simulation

FY 1996 Determined suitability of aluminum gallium arsenide mobility models in commercial device simulators.

FY 1997 Investigate with industry partners methods for measuring mobilities in aluminum gallium arsenide and other compound semiconductor devices; Investigate influence of the mobility models on device simulation.

FY 1998 Investigate the development of benchmarks for determining suitability of effective intrinsic carrier concentration in device simulators for compound semiconductor devices; Use simulator that accounts for quantum mechanical tunneling to calibrate and benchmark simulators for ultra-thin layered structures.

5. Develop metrology for calibration and benchmarking of process simulation parameters

FY 1987-95 Developed ion transport simulation code and used to investigate secondary ion mass spectrometry and sputtering. Developed dopant diffusion simulation capability including implant damage; Formed Ion Implant Users Group.

FY 1996 Initiated and organized first national ion implant users group meeting; Reported on simulation of boron-10 implants for SRM design and sensitivity analysis.

FY 1997 Calibrate implant models in SUPREM4 process simulator using Monte-Carlo ion implant simulator; Investigate methods to benchmark SUPREM4 for boron diflouride implant including anneal; Investigate methods of simulating low-energy boron including backscattering and sputtering using SUPREM4 and calibrate using TRIM.

Metrology for Devices and Packages

(Project refocused to better meet industry needs - see new project sheet "Metrology for Simulation and Computer-Aided Design")

Project Leader: Allen R. Hefner

Staff: 5.0 Professionals, 1.0 Graduate Research Fellow, 1.0 Visiting Scientist, 0.1 Faculty Hire

Funding level: $1.1 M

Funding sources: NIST (75%), Other Government Agencies (25%)

Objective: Promote the efficient and reliable application of semiconductor devices by: developing advanced device and package characterization methods; metrology, data, and techniques for advanced device and system simulation; and support of and participation in national and international standards and industry organizations.

Background: The project addresses needs at the boundary between the device and the device in its application. The National Technology Roadmap for Semiconductor identifies integration of component-level electrical, thermal, and mechanical models for semiconductor devices and packages, and the availability of calibrated and easy-to-use technology computer-aided-design tools for device, process, and circuit simulation as areas requiring development and support to achieve the 15-year goals of the Roadmap. Structures and operation of devices are advancing rapidly where high performance and high efficiency are required. Advanced device electrical and thermal characterization procedures and validation of models used in computer aided design tools have not kept pace with the application of the new device types. In addition, the high-speed, high-current density, and high-power dissipation levels of advanced circuits and devices have increased the importance of microelectronic package electrical and thermal characteristics to overall system performance.

Current Tasks:

1. Develop package thermal characterization and analysis techniques

FY 1989	Completed a five-year program for providing the semiconductor industry with methods for thermal characterization of microelectronic packages; three test methods finished this year, six overall.
FY 1990	Developed transient thermal model for ultra-small structures to aid in defining practical limits for the electrical measurement of temperature for these structures. Structures less than about 50 micrometers on a side represent a lower practical limit.
FY 1991	Demonstrated that for gallium arsenide devices on a silicon substrate, the thermal spreading resistance in the thin gallium arsenide layer beneath the device significantly increases the total thermal resistance of the device.

FY 1992	Completed development of a compact thermal component modeling procedure (including chip, package, and heatsink) designed for use in advanced electro-thermal system simulators.
FY 1993	Assisted Sandia Laboratories in the evaluation of a packaging thermal test chip designed at Sandia.
FY 1994	Extended NIST TXYZ thermal analysis program to include multilayer, microelectronic structures.
FY 1995	Developed in-house capability for computational fluid dynamics (CFD) simulations using FLOTRAN (packaged with ANSYS) and proprietary code from the University of Maryland.
FY 1996	Completed CFD simulations and measurements of package array in a 'lap-top-like' enclosure to assess package modeling and characterization issues important for this type system; Determined applicability of micromachined, thermally isolated heaters for use as *local* heat flux sensors for packages.

2. Develop metrology for microelectronic packaging and assembly

FY 1988	Evaluated status of superconductors for packaging applications. Concluded that materials are evolving too rapidly to allow a reasonable effort.
FY 1989	Completed research on two-dimensional modeling of gold-aluminum intermetallic diffusion under various bonding conditions.
FY 1990	Published a comprehensive reference book on wire bond yield and reliability resulting from a long-term program at NIST.
FY 1992	Developed procedure to improve high yield and fine pitch wire bonding.
FY 1993	Recommended practice for bonding and metallization for use on infrared detectors for Geostationary Operational Environmental Satellite.
FY 1994	Participated in a Department of Commerce 232 trade investigation into imported electronic packages.
FY 1995	Completed setting up the experimental apparatus to measure the 60 hertz vibration modes of capillary bonding tools; Preliminary measurements have been made; Completed study of wire bonding to multichip modules and other soft substrates; Performed finite element study of wire bonding to soft substrates. (Collaboration with Computing and Applied Mathematics Laboratory)
FY 1996	Finished second edition of comprehensive reference book “Reliability and Yield Problems of Wire Bonding and Microelectronics;” Consulted with industry on wire bonding production problems.

3. Develop and establish metrology for power semiconductor devices

FY 1989	Constructed nondestructive device failure test system capable of determining power device failure limits with current up to 100 amperes and voltages to 2000 volts.
FY 1990	Organized and hosted 6th NIST/IEEE Power Semiconductor Devices Workshop. The IEEE is an engineering professional society called the Institute of Electrical and Electronic Engineers.
FY 1992	Established failure limits and identified failure mechanisms for bipolar-mode field-effect transistor; Discovered unexpected tendency for this device to be thermally unstable.
FY 1994	Provided technical support and guidance to a flat-panel display manufacturer; Characterized power failures in their system that led to a redesign.

FY 1996	Provided technical support and guidance on integration of design aspects and concurrent engineering to U. S. Navy's Power Electronic Building Block (PEBB) Program.

4. Develop device modeling and metrology for system level simulation

FY 1988	Developed first analytic model for the Insulated Gate Bipolar Transistor (IGBT) and demonstrated its usefulness in describing device/circuit interactions.
FY 1989	Extended IGBT model to include transients and demonstrated the need to use nonquasi-static theory to describe transient behavior.
FY 1990	Incorporated IGBT model into a commercial circuit simulator in collaboration with a U.S. company.
FY 1991	Developed, verified, and documented parameter extraction measurement procedures for IGBT circuit simulator implementation.
FY 1992	Completed development of dynamic electro-thermal model for the IGBT.
FY 1993	Completed implementation of the 'buffer layer' IGBT model into the commercial circuit simulator.
FY 1994	Formed the NIST Model Validation Working Group.
FY 1995	Completed computer framework for technology computer-aided design within the Group.
FY 1996	Continued leadership role in Model Validation Group; Developed IGBT model validation procedures, organized IGBT model validation task group meeting; Investigated features required for a comprehensive model development platform.

5. Develop physics for device-level modeling and simulation

FY 1989	Established the limitations of conventional device physics, based on uniform materials, for devices that have increasing doping gradients for dimensions to 0.1 micrometer.
FY 1990	Performed first principle calculations for changes in conduction and valence bands that occur as a result of either high doping or carrier densities or both in gallium arsenide and silicon; Calculated majority- and minority-carrier mobilities in heavily doped gallium arsenide and compared with experiments; Calculations included in device simulators.
FY 1991	Verified device physics for gallium arsenide heterostructure bipolar transistors and results in a more accurate HBT simulator.
FY 1992	Calculated majority- and minority-carrier mobilities in heavily doped silicon and compared with experiments; Calculations included in device simulators.
FY 1995	Calculated majority- and minority-carrier mobilities in heavily doped aluminum gallium arsenide as functions of aluminum concentration and doping densities and compared with experiments.

Silicon-on-Insulator Metrology

Project Leader: Peter Roitman

Staff: 1.0 Professional, 1.0 Technician, 1.0 Grantee/student

Funding level: $0.4 M

Funding sources: NIST (65%), Other Government Agencies (35%)

Objective: Develop advanced measurement methods for defect detection in silicon-on-insulator material; develop silicon-on-insulator material for insertion in silicon integrated circuit manufacturing; provide expertise to other government agencies regarding silicon-on-insulator programs.

Background: Silicon-on-Insulator (SOI) wafers have advantages over bulk silicon for isolation and process simplicity, for short channel device performance, and for applications involving low power, high temperature, high speed, integrated power, and radiation hardness (including soft errors). However, several different types of defects have been identified which are unique to these materials and the conditions of their fabrication. Identification of defect types and development of characterization techniques suitable to SOI are prerequisites to both the minimization of the number of defects, through process control, and to the commercial acceptance of the material. The primary focus of this project has been on the development of characterization techniques and methods, to facilitate material improvement to the point of commercial viability. Also, several government agencies have been involved in programs to develop SOI materials, due to particular requirements of their mission, and the project has interacted with them.

Current Tasks:

1. Develop characterization techniques for SOI material

FY 1988	Evaluated the many existing SOI technologies. SIMOX (formation of a buried oxide by high dose ion implantation) was chosen as the most promising and, hence, the focus of the project. Completed construction of high-temperature furnace essential for SOI (SIMOX) fabrication; Completed secondary ion mass spectrometry and Rutherford backscattering round robin to calibrate impurities of importance in SOI material; Developed the use of electron channeling patterns to nondestructively measure oxide precipitates and silicon dislocations.
FY 1989	Began work on transmission electron microscopy (TEM) and materials analysis. (Collaboration with Arizona State University) TEM cross-sections used to show effect of annealing temperature and ambient on oxide precipitates and dislocations in the silicon film; Established limits of detectability for electron channeling pattern technique for defect detection; Developed etch pit with scanning-electron-microscope counting technique for low-density defects in the silicon film; Developed a complementary metal oxide-semiconductor (CMOS) on SIMOX process at NIST. Designed two CMOS on SIMOX test chips.

FY 1990	Established 1300 °C as minimum temperature for dissolution of oxide precipitate complex. Industry adopted 1310 °C or 1325 °C as standard for SOI (SIMOX) processing. Established 600 °C as the minimum implant temperature required for low-defect-density silicon films; Developed and experimentally verified a theoretical model for the analysis of the capacitance-voltage curve of a complete SOI stack; Demonstrated the improvement in spectral fit which occurs as the ellipsometric model is made increasingly physical; Completed NIST3A4 mask set for CMOS on SIMOX test chip. Processed initial lots at NIST.
FY 1991	Proved that high-leakage currents in buried oxides were due to "pipes" of silicon caused by particles on the surface of the wafer during the SIMOX oxygen implant; Transferred potassium hydroxide etch technique and results to industry. Particle problem largely eliminated by industry. Developed modified Secco/HF etch for reliable delineation of silicon defects; Transferred technique to industry (has become industry standard); Proved existence of large numbers of silicon dangling bond defects uniformly distributed through buried oxide by spin resonance capacitance voltage, etc.
FY 1992	Showed reduction in silicon defect density by annealing sequence; Identified high-field conduction mechanisms for buried oxides. CMOS on SIMOX processing at NIST ended.
FY 1993	Demonstrated the effect of nitridation of the buried oxide, using nitrogen, ammonia, and nitrous oxide ambients; Explained the full mechanism for formation of silicon defects in high dose SIMOX. Demonstrated the defect types present in bonded silicon wafers (BESOI) using the techniques developed for SIMOX. Showed the experimental physics of the formation of silicon precipitates in the buried oxide at low and medium dose.
FY 1994	Demonstrated the effect of high-temperature annealing in the range of 1300 °C to 1350 °C on silicon defect structure and interface roughness. Explained the mechanism for formation of silicon defects in low and medium dose SIMOX.
FY 1995	Showed leakage current in low dose SIMOX due to effects of silicon precipitates.
FY 1996	Developed etch technique for silicon precipitates in SIMOX buried oxides and applied technique to experimental low and medium dose material; Determined effect of dose on precipitate density; Started development of novel process for low defect, low dose SIMOX.
FY 1997	Develop and characterize processes for low dose SIMOX material; Characterize bonded and thick silicon SIMOX material.

2. Provide technical support and assist in oversight of SOI projects for other agencies of the U.S. government

FY 1988-94	The primary driver for SOI development in the U.S. was the need for radiation-tolerant electronics for satellite applications. The Defense Nuclear Agency and the Strategic Defense Initiative Office were the agencies primarily concerned. The project participated in contract reviews and planning activities with these agencies.
FY 1995-97	The application driver for SOI development changed to low power, battery-operated, portable electronics. The Defense Advanced Research Projects Agency initiated a program in Low Power Electronics. The project is heavily involved with the planning and management of this program.

Metrology for Process and Tool Control

Project Leader: Michael W. Cresswell

Staff: 2.5 Professionals, 0.2 Guest Scientist, 1.4 Technician

Funding level: $0.9 M

Funding sources: NIST and OMP (84%), Other Government Agencies (16%)

Objective: Develop advanced test-structure-based electrical measurement methods and related reference materials for industry with a primary emphasis on overlay and linewidth metrology and calibration; interact with standards groups to provide a metrology base for the semiconductor tool industry.

Background: Succeeding generations of integrated circuits are characterized by the widths of the narrowest lines that are replicated during the wafer-fabrication process. Control of gate length during wafer fabrication is a key factor affecting device performance and overlay control is essential for economically viable manufacturing. Reliable metrology for monitoring these parameters has been identified in the National Technology Roadmap for Semiconductors as a central requirement for maintaining the necessary fabrication-process control. The demands on gate-length and overlay metrology are increasing as the complexity of integrated circuits increases from one generation to the next. Of the several techniques of linewidth-control and overlay metrology, only electrical test structures currently have a measurement reproducibility that conforms with future projected error budgets.

Current Tasks:

1. Develop metrology for electrical linewidth (electrical critical dimension)

FY 1988	Documented and extended statistical model and error analysis for characterizing the performance of a submicrometer lithography based on electrical test structure measurements.
FY 1989	Demonstrated lithography-process diagnosis using rule-based analysis of spatial linewidth variations extracted from multiple design-rule structures replicated in polysilicon on 100 millimeter wafers.
FY 1990	Developed and demonstrated guidelines for characterizing electron-beam pattern-generator linewidth control by extracting electrical linewidth measurements from electrical test structures.
FY 1991	Compared measurements extracted from scanning electron microscope measurements and measurements using electrical cross-bridge structures having design linewidths to 0.3 micrometers.
FY 1992	Applied principles of empirical tap-width correction to linewidth extraction from cross-bridge test structures having bridge lengths shorter than 10 micrometers.

FY 1993	Demonstrated static measurement precision of 1 nanometer for lines with 350 nanometer design linewidths.
FY 1994	Compared measurements of lines having drawn widths from 0.35 micrometers to 1.5 micrometers by a range of metrological techniques including optical, electrical, and scanning electron microscopy.
FY 1995	Showed agreement to within 10 nanometers for several materials for electrical linewidth and the Molecular Measurement Machine (M^3) when operating in scanning-tunneling-microscope mode. Optical and electrical linewidth measurement differences are on the order of 100 nanometers.
FY 1996	Developed first electrical linewidth test structures with atomically-planar sidewall vertical features having known sidewall slopes in monocrystalline material; Tested to identify origins of critical dimension metrology methods divergence.
FY 1997	Develop electrical test structures having features with atomically-planar vertical sidewalls, which will enable co-calibration by transmission optical and scanning electron microscope metrology; Design, fabricate, and test potential future reference materials for lithography using light with a wavelength of 193 nanometers.
FY 1998	Fabricate and evaluate features having known sidewall slopes on silicon-on-insulator material.

2. Develop metrology for electrical overlay

FY 1991	Demonstrated novel electrical test-structure based on the linear voltage-dividing potentiometer for the determination of accuracy and precision of feature placement by primary-pattern-generator systems; Demonstrated sub-15 nanometers electrical metrology with commercially-available test equipment.
FY 1992	Introduced voltage taps extending across the current-carrying bridge for feature-placement metrology, thereby substantially eliminating process-induced shifts resulting from asymmetrical inside-corner rounding.
FY 1993	Demonstrated the dynamic precision of electrical overlay test structures to be 1.5 nanometers, and their uncertainty less than 10 nanometers, by comparing electrical measurements with those made by the NIST Line-Scale Interferometer.
FY 1994	Developed and obtained patents for improved optical overlay-instrument calibration substrates and for electrical certification of graduated scales.
FY 1995	Designed, fabricated, and electrically tested substrates at multiple sites co-inspected by the NIST Line-Scale Interferometer.
FY 1996	Presented paper at SEMATECH to invited industry audience on new hybrid optical-electrical test structure to facilitate pixel-calibration of optical overlay systems; Initiated a consortium with industry to evaluate new overlay-metrology methods; Developed plan to implement mix-and-match overlay metrology for 193 nanometer lithography system.
FY 1997	Incorporate electrical null-detectors into hybrid optical-electrical test structures to enable fabrication-process corrections of both tool- and wafer-induced shift.
FY 1998	Fabricate structures for coordinate measurement system and optical overlay tool calibration using microelectromechanical systems technology.

3. Promote development of X-ray metrology infrastructure

FY 1992	Led development of consensus among eight DoD industry contractors for mask-support ring dimensional standards for DARPA X-ray lithography based on finite-element analysis of residual distortion for beam-line applications.
FY 1993	Extended capability of mask-support ring dimensional standard for point-source systems.
FY 1994	Drafted initial international voluntary standard for X-ray mask configurations and chaired video-conference between U.S.-industry representatives and a Japanese task force on convergence between North American and Japanese standards.
FY 1995	Prepared revisions to draft of U.S. standard and obtained concurrence with the Japanese on almost all major points previously under contention.
FY 1996	Developed further agreement between U.S. industry and Japan on final draft of new international voluntary X-ray mask standard.
FY 1997	Submit revised draft of the X-ray mask standard agreed to by both Japanese and American companies to SEMI balloting process.
FY 1998	Provide consultation to international X-ray community on standard non-circular masks.

4. Initiate Back End of Process Characterization

FY 1994	Identified potential process control issues; Obtained design rules.
FY 1995	Designed contact resistor test strip and a back end of process test chip (NIST 23); Delivered designs to contractor.
FY 1996	Tested and evaluated test strip and provided results to collaborator; Task terminated at conclusion of ATP contract period of performance.

Interconnect Reliability Metrology

Project Leader: Harry A. Schafft

Staff: 2.2 Professionals, 0.2 Technicians

Funding level: $0.5 M

Funding sources: NIST and OMP (89%), Other Government Agencies (11%)

Objective: Provide domestic manufacturers with test structures, test methods, and diagnostic procedures for improving the reliability of metal interconnects used in integrated circuits and promote the use of a building-in reliability approach within the semiconductor industry.

Background: Interconnect reliability in integrated circuits continues to be a topic of intense interest, as evidenced by an increasing number of publications on the subject each year. This intense interest is the result of the planned aggressive scaling of integrated circuits and the need for ever greater product reliability, as expressed in the National Technology Roadmap for Semiconductors. The key underpinning of efforts in this area is the development of the measurement tools and standards to facilitate the goals of the industry.

Current Tasks:

1. Develop electromigration standards and metrology methods

FY 1988	Submitted drafts of three electromigration-related documents for balloting as standards to the American Society for Testing and Materials (ASTM), a U.S. voluntary standards organization, through its Subcommittee F1.11 on Quality and Hardness Assurance; Developed a wafer-level test station for making steady state and pulsed electromigration stress tests at temperatures as high as 300 °C; Initiated pulsed stress electromigration testing; Completed collaborative effort with a large semiconductor company and the NIST Statistical Engineering Division on the statistics of electromigration testing.
FY 1989	Discovered a new measurement interference for highly accelerated electromigration stress tests; Developed a new, state-of-the-art wafer test station to perform dc and pulsed electromigration stress tests at room temperature to over 300 °C; Designed a test chip (NIST-2) for use in optimizing the procedure for measuring the thermal conductivity of thin, dielectric films and for conducting pulsed and dc electromigration stress tests.
FY 1990	Demonstrated that the pulsed enhancement of electromigration is dependent on current density; Guided the adoption of three ASTM standards for electromigration that represent first standards for the characterization of interconnect metallizations.
FY 1991	Completed study of power lognormal distribution for modeling electromigration failure times which predicted much lower early reliability values for metallizations; Designed a test chip (NIST 13) to evaluate validity

of power lognormal distribution for describing electromigration-related failures.

FY 1992 Showed that the classical electromigration stress test can be used at ultra-high stress levels; Discovered an unusually large enhancement of conductor lifetime under pulsed dc stress that depends on current density and oxide thickness.

FY 1993 Characterized the power lognormal distribution for modeling electromigration failure-time data which include a quantification of the length dependence and of a worst-case estimate of the early reliability of conductor lines.

FY 1994 Initiated work on a new package-level electromigration test station; Began interlaboratory electromigration comparison.

FY 1995 Completed initial draft of a Joint Electron Device Engineering Council (JEDEC) standard for calculating the acceleration factors for electromigration for JEDEC Committee 14.2; Completed extensive revisions to ASTM F 1261, Standard Method for Determining the Average Electrical Width of a Straight,Thin-Film Line, including a bias and precision statement (from the results of an interlaboratory experiment) for subcommittee F1.11.

FY 1996 Completed revision of ASTM Standard Guide F 1259 for designing electromigration test structures and of ASTM Standard F 1260 for characterizing electromigration; Explored use of Matthiessen's rule to measure electrical thickness and area of copper interconnects.

FY 1997 Complete JEDEC standard for calculating the model parameters for electromigration. Complete JEDEC guide for standard probe pad sizes and layouts for wafer-level electrical testing. Design test chip for conducting second electromigration interlaboratory experiment to determine the precision of the ASTM standard method for characterizing electromigration.

FY 1998 Complete revision of ASTM standard method for characterizing electromigration and designing test structure in collaboration with Industrial Advisory Group.

2. Develop thin-film characterization methods

FY 1988 Initiated work on developing techniques for measuring the thermal conductivity of thin-film dielectrics used in very large scale integrated circuits.

FY 1989 Reported results of thermal conductivity measurements of thin-film silicon dioxide.

FY 1990 Began a study to evaluate the use of Matthiessen's Rule for electrically determining the thickness of aluminum-based metallizations.

FY 1991 Explored use of sophisticated mechanical probe to evaluate electrical method for measuring metal film thickness.

FY 1992 Began exploration of a scanning electron microscope as means to evaluate electrical method for measuring metal film thickness.

FY 1993 Developed method for making cross sections of metal-film specimens for SEM examinations using a scanning electron microscope.

FY 1994 Refined use of Matthiessen's rule to measure thickness of metal films by an electrical method; Demonstrated agreement with calibrated measurements. (Collaboration with Rensselaer Polytechnic Institute) Measured thermal conductivity of different types of oxide films.

FY 1995	Documented the use of Matthiessen's rule for determining aluminum film thickness and line cross-sectional area from electrical resistance measurements.
FY 1996	Completed first phase of interlaboratory experiment to assess reproducibility of thickness measurements; initial results show good agreement.
FY 1997	Complete selective thermal conductivity measurements of silicon dioxide thin films and modeling experiments to improve characterization; Continue an interlaboratory experiment to verify the reproducibility of thickness measurements of thin metal film using Matthiessen's rule.
FY 1998	Complete draft of a JEDEC standard for determining the electrical thickness of thin metal films using resistance measurements.

3. Develop improved temperature coefficient of resistance (TCR) metrology

FY 1990	Prepared a draft standard on the measurement of the TCR of interconnect metallizations in response to a JEDEC request.
FY 1991	Developed JEDEC standard based on previously NIST-developed standard for measuring and using metallization TCR at request of JEDEC.
FY 1992	Revised the Electronic Industries Association Joint Electron Device Engineering Council Standard on measuring and using TCR of a metallization.
FY 1993	Developed a surface-temperature probe for improved temperature measurement capability, used as a calibration source in second interlaboratory experiment.
FY 1994	Completed first draft of Bias and Precision Statement for JEDEC TCR standard (JESD33).
FY 1995	Documented the results of the JEDEC interlaboratory experiment for TCR, joule heating, linewidth, and hot-chuck measurements; Authored revised bias and precision section for JEDEC standard JESD33 (Standard Method for Measuring and Using the TCR to Determine the Temperature of a Metallization Line) for JEDEC.
FY 1996	Revised standard JESD33 distributed by JEDEC; News release announcing revised standard prepared by NIST. Task completed.

4. Promote Building-in Reliability (BIR) infrastructure development

FY 1989	Developed plans for highlighting the critical changes needed for industry to meet future reliability and market-entry demands.
FY 1990	Developed technical program for the International Reliability Physics Symposium (IRPS) 1990 that introduced new focus for the Symposium: Building-In Reliability.
FY 1991	Promoted building-in reliability approach for industry by delivering invited keynote talks at IRPS, European Symposium, Reliability of Electron Devices, Failure Physics, and Analysis (ESREF) Workshop sponsored by the Semiconductor Research Council.
FY 1992	Took lead role at industry request, in developing technical advisory group from the industry for continuing an important workshop for wafer level reliability.
FY 1993	Developed a management structure for the Wafer Level Reliability Workshop to enable it to be a self-sustaining entity.

FY 1994	Began plans for the preparation of an invited presentation on BIR at a reliability conference in Budapest and of an invited paper on the same subject for a special issue of the Microelectronics and Reliability Journal.
FY 1995	Prepared three papers to promote a more rapid transition from a testing-in-reliability to a building-in-reliability approach in the semiconductor industry.
FY 1996	Worked with members in the semiconductor industry to develop plans and to organize a seminar on building-in reliability (BIR) for customers of semiconductor vendors.
FY 1997	Provide leadership to U.S. industry in the area of BIR; Serve as editor of e-mail newsletter for BIR newly formed Special Interest Team; Publish invited paper on BIR in *Microelectronics and Reliability* with industrial co-authors; Make plans for other seminars and papers with industrial colleagues.

Dielectric Reliability Metrology

Project Leader: John S. Suehle

Staff: 1.8 Professionals, 1.0 Post Doc, 0.2 Technicians

Funding level: $0.5 M

Funding sources: NIST and OMP (62%), Other Government Agencies (38%)

Objective: Provide domestic semiconductor manufacturers with improved test structures, test methods, models, and novel sensor-based metrology for improving device reliability and monitoring tool performance and manufacturing processes.

Background: The domestic semiconductor industry is aggressively scaling gate oxides in microelectronic devices to achieve higher chip performance and packing density. Reduced time-to-market and new oxide processes require fast and effective reliability characterization techniques. Physically correct models and tests to predict reliability of thin oxides under dc and ac operating conditions are needed. As the semiconductor industry rapidly builds capacity to meet worldwide demand for their products, national standards are required to characterize dielectric integrity for plant-plant and vendor-customer evaluation. Finally, it has been recognized by the National Technology Roadmap for Semiconductors that reliability and novel in-situ process sensors are required to manufacture competitive, cost-effective semiconductor products and improve manufacturing process and tool control.

Current Tasks:

1. Develop dielectric reliability standards and metrology methods

FY 1991	Organized, designed, and conducted an international Joint Electron Device Engineering Council (JEDEC) interlaboratory experiment (with nine labs) to evaluate two JEDEC-proposed dielectric breakdown test methods involving current- and voltage-ramp stresses; Analyzed the measurement results and found good agreement; Modified a commercial hot chuck and controller to enhance capabilities for making measurements of test-line temperatures repeatable at the wafer level.
FY 1992	Developed a document for Wafer-Level Testing of Thin Dielectrics which was accepted as Electronic Industries Association (EIA)/JEDEC Standard JESD35.
FY 1993	Presented first Time Dependent Dielectric Breakdown (TDDB) data at temperatures up to 400 °C. Before this time it was not known if silicon dioxide could be used for high temperature electronics.
FY 1994	Improved understanding of TDDB in thin silicon dioxide films by verifying the electrical field dependence of the mechanism at low stress electrical fields (4×10^6 V/cm) by using novel high-temperature wafer-level probe station.
FY 1995	Revised and had approved by committee ballot two new JEDEC standards: "General Guidelines for Designing Test Structures for the Wafer-Level

Testing of Thin Dielectrics" and "Addendum on Test Criteria for the Wafer-Level Testing of Thin Dielectrics." The first standard has been approved by JEDEC Council. Awaiting Council approval on second standard. Demonstrated differences of electric field and temperature dependence of TDDB for bimodal failure distributions; Performed TDDB characterization of 9 to 22 nanometer thick oxides with unipolar and bipolar pulsed bias stress over wide range of temperature and electric field.

FY 1996 Coordinated joint JEDEC-ASTM (American Society for Testing and Materials) working group to develop standard voltage ramp gate oxide integrity tests; Studied charge-trapping characteristics of thin oxides when subjected to dc or pulsed voltage stress.

FY 1997 Study TDDB field and temperature dependence of ultra-thin dielectrics with thicknesses less than 10 nanometers; Conduct nine-laboratory round robin to evaluate new ASTM-JEDEC V-ramp Test for ultra-thin oxides.

FY 1998 Develop improved lifetime model for gate oxides less than 5 nm thick and operating under either time invariant or varying voltages operating under dc and ac conditions.

2. Develop micro-hotplate gas sensor

FY 1992 Filed three patents on the micro-hotplate and tin oxide gas sensor. (Collaboration with the NIST Chemical Science and Technology Laboratory [CSTL]).

FY 1993 Developed the first monolithic tin oxide gas sensor realized with commercial processing by silicon micromachining. (Collaboration with CSTL)

FY 1994 Conducted a study on the reliability of micromachined polysilicon heaters when subjected to constant current stress. High-gain Optical Beam Induced Current (OBIC) imaging was used for the first time to examine the structural effects of stress on the devices. The results indicate that the resistance drift exhibited by the resistors during stress is due to electromigration of the dopant atoms.

FY 1995 Designed a new micro-hotplate chip, NIST21, and had fabricated by the Microelectronics Research Laboratory (NSA). The devices have tungsten metallization for improved heater stability and reliability.

FY 1996 Demonstrated four-element gas sensor array for compositional gas analysis with CSTL.

FY 1997 Demonstrate chemical sensor prototype in industrial application to monitor manufacturing process of titanium matrix composites.

FY 1998 Complete development of multi-element chemical sensor array that incorporates several different metal-oxide sensing films.

Micro-Electro-Mechanical Systems (MEMS)

Project Leader: Michael Gaitan

Staff: 1.6 Professionals, 1.7 Guest Scientists, 0.5 Graduate Research Fellows, 0.2 Technicians, 0.2 Faculty Hire

Funding level: $0.5 M

Funding sources: NIST (44%), Other Government Agencies (56%)

Objective: Provide domestic industry with infrastructure for improved accessibility to MEMS manufacturing, develop techniques for MEMS device design and characterization, performance testing, and parameter extraction, and provide novel MEMS-based devices for metrology applications.

Background: The emerging technology of Micro-Electro-Mechanical Systems (MEMS) utilizes mechanical structures, fabricated in an integrated-circuit-based process, to miniaturize mechanical elements and perform new functions. Applications for this technology include pressure sensors, inertial sensors, gas and fluid regulation and control, process control, optical switching, and mass data storage. Market studies forecast a worldwide market of nearly $14 billion by the year 2000, enabling almost $100 billion in new or improved systems. Domestic industrial needs for MEMS manufacturing include the integration of electromechanical structures with microelectronic circuits and the development of characterization techniques of electromechanical properties that relate to device geometry and the manufacturing processes. Meeting this objective will enable industry to manufacture competitive, cost-effective products, improved manufacturing processes, device performance, and device reliability. In addition, MEMS devices have applications for in-situ semiconductor fabrication process monitoring and control, a critical element recognized by the National Technology Roadmap for Semiconductors, as a key step required for the next generation of semiconductor devices.

Current Tasks:

1. Develop thermal flat-panel display

FY 1991	Initiated a program to develop a complementary metal oxide-semiconductor-(CMOS-)based thermal flat-panel display; Demonstrated the concept of fabricating micro-heating elements through a commercial CMOS process; Designed, fabricated through the University of Southern California/Information Sciences Metal Oxide Semiconductor Informational Services (MOSIS), performed silicon micromachining on CMOS chips, and tested the elements for applications as infrared emitters or pixels in a thermal flat-panel display.
FY 1992	Demonstrated the concept of using micro-heating elements as pixels in a small size thermal (infrared) flat-panel display; Designed, fabricated, and tested a 4 x 4 infrared pixel array for application as a thermal flat-panel display.

FY 1993	Designed, fabricated, and tested a 16 x 16 infrared pixel array; Interfaced the array to a computer and a video interface; Collected thermal images of the output of the display; Designed 64 x 64 and 128 x 128 infrared (IR) pixel array thermal flat-panel displays.
FY 1994	Completed the demonstration of concept of using micro-heating elements, fabricated in a commercial foundry process, to fabricate thermal flat-panel displays; Fabricated 64 x 64 and 128 x 128 infrared pixel array thermal flat-panel displays; Completed testing of 64 x 64 and 128 x 128 infrared pixel arrays.
FY 1995	Initiated a 3-year program to build prototype thermal flat-panel displays. (Collaboration with industrial partner)
FY 1996	Worked with industrial partner to design, fabricate, and test 64 x 64 pixel array prototype thermal display integrated circuits to be inserted in optical projection system for the first phase field demonstration; Initiated work to design and fabricate 128 x 128 pixel array prototype thermal display integrated circuits for the second phase of the task.
FY 1997	Complete second generation design for a 64 x 64 pixel array display, submit for fabrication, and test the fabricated array for operation; Complete designs of 128 x 128 pixel array prototype thermal display integrated circuits to be inserted in the optical projection system.
FY 1998	Complete a working demonstration thermal display unit with projection optics in collaboration with industrial partner.

2. Develop microwave power sensor

FY 1991	Began development of a CMOS equivalent to the multijunction thermal converter fabricated in the Semiconductor Process Laboratory. (Collaboration with the Electricity Division) Initial designs sent to the MOSIS service for fabrication.
FY 1992	Fabricated improved designs of thermal converter elements and tested ac/dc conversion accuracy to 1 megahertz with conversion error under 200 parts per million.
FY 1993	Initiated a program to develop a high-precision low-cost RF and microwave power sensor to 10 gigahertz; Fabricate transmission lines and power sensors; Began the CRADA with industrial partner.
FY 1994	Demonstrated the concept of fabricating silicon micromachined microwave transmission lines in CMOS technology; Tested the transmission line elements to 20 gigahertz and demonstrated the benefits of silicon micromachining to reduce the attenuation of the lines.
FY 1995	Demonstrated the concept of fabricating silicon micromachined power sensors and coupling these devices to the CMOS transmission lines; Tested the CMOS silicon micromachined microwave power sensors to 20 gigahertz.
FY 1996	Developed a working prototype microwave power meter in collaboration with industrial partner; Incorporated the transmission line elements and the microwave power sensors with circuits on an IC chip and test and characterize the elements and circuit performance.
FY 1997	Characterize polysilicon load element and investigate techniques to control its stability for accurate power measurement; Begin integration of analog-to-digital converter and input/output electronics on power sensor integrated circuit and test and characterize the elements and circuit performance.

FY 1998	Complete the integration of analog-to-digital converter and input/output electronics on the power sensor integrated circuit and test and characterize the elements and circuit performance.
FY 1999	Complete a working demonstration hand-held microwave power sensor unit based on the CMOS foundry-compatible microwave power sensor technology, in collaboration with the industrial partner.

3. Develop electromechanical test structures/promote MEMS infrastructure

FY 1992	Designed test structures to determine design rules needed for design and fabrication of CMOS-compatible MEMS devices.
FY 1993	Submitted a design library to MOSIS of CMOS-compatible MEMS devices and test structures. MOSIS announced its official support of CMOS compatible MEMS as a result of this effort.
FY 1994	Designed a set of test chips in collaboration with the Massachusetts Institute of Technology, Case Western Reserve University, and the University of California at Berkeley, and fabricated through the Microelectronics Center/North Carolina MUMPs service that contained electromechanical test structures. A test chip was also designed in collaboration with others at NIST.
FY 1995	Installed interferometric microscope system for measurement of deflections of the electromechanical test structures; Began measurements of the test structures.
FY 1996	Worked with the NIST MEMS Strategic Planning Committee to hold a Strategic Planning Workshop in November 1995 in an effort to determine whether there is a need for a NIST-wide MEMS program; Completed characterizations of cantilever and fixed beam MEMS test structures; Competence proposal submitted and review held.
FY 1997	Continue work on MEMS-based test structure development; Focus efforts on developing models that describe the fixed-fixed (attached at both ends) beam data; Work with MOSIS and the MEMS technical community to correct run-to-run uniformity problems with the open design rule and to attempt CMOS foundry-compatible process through alternative technologies; Make plans for future growth of the activity based on the results of the competence review.

Plasma Chemistry - Plasma Processing

Project Leader: James K. Olthoff

Staff: 1.5 professionals, 1.0 guest scientist

Funding level: $0.4 M

Funding sources: NIST and OMP (100%)

Objective: To aid the semiconductor industry in the characterization of discharges used in plasma processing. Specifically by investigating 1) the effects of surface charging, 2) the chemical composition of capacitively- and inductively-coupled rf plasmas, 3) the performance of ion energy analyzers for use as plasma diagnostics, 4) the effect of ion-molecule collisions on the ions striking surfaces exposed to the plasma, and 5) fundamental collision data required for analysis of plasma processing data.

Background: The Electricity Division's work in plasma processing began in 1989 as an outgrowth of NIST's work in gaseous dielectrics. Initial work involved the evaluation of a mass spectrometer with an ion energy analyzer as a plasma diagnostic for SEMATECH. Subsequent research has been supported primarily by the EEEL Office of Microelectronics Programs under the National Semiconductor Metrology Program, and has emphasized the characterization of diagnostic devices and validation of theoretical models. In the past 5 years NIST has become a leader in the development of “reference” discharges for use in these studies, including GEC rf Reference Cells with capacitively- and inductively-coupled sources, and a Townsend discharge cell. A "GEC rf Reference Cell" is a test chamber, "cell", in which the plasma is sustained by applying a high frequency electric field, "rf". The GEC refers to the Gaseous Electronics Conference where the need for such a standard test system was first discussed. Application of a wide range of diagnostic measurements, (electrical, mass spectrometric, ion energy analysis, optical emission and laser-induced fluorescence) to these well-characterized discharges, allows the accumulation of baseline plasma data necessary to confirm the performance of both the measurement techniques and the predictive models used to describe the discharge.

Current Tasks:

1. Application of mass spectrometric, ion energy diagnostics to discharges

FY 1989	Interacted with SEMATECH concerning need for characterization and calibration of a mass spectrometer/ion energy analyzer and a Langmuir probe.
FY 1990	Fabricated and brought to full operation GEC rf reference cell with optical, mass spectrometric, and electrical diagnostics.
FY 1991	Characterized mass spectrometer/energy analyzer for use as a real time diagnostic in rf production reactors; Sent results to SEMATECH for publication as a SEMATECH report.

FY 1992	Installed improved mass spectrometer/ion energy analyzer system to GEC Cell; Measured ion energy distributions in argon, argon/oxygen, and argon/helium mixtures and correlated with electrical and optical measurements.
FY 1993	Measured effects of trace impurities, such as oxygen or water, on electrical characteristics of argon discharges.
FY 1994	Performed comprehensive studies (including mass spectrometric, ion energies, optical emission, and electrical) of rf discharges in hydrogen and argon/hydrogen; Performed preliminary ion energy measurements in dc Townsend discharges.
FY 1995	Edited special journal issue dedicated to research performed on GEC rf Reference Cells; Constructed new inductively coupled GEC rf cell.
FY 1996	Completed investigation of rf discharges in sulfur hexafluoride; Completed investigation of ion energy diagnostic measurements for dc Townsend discharges in argon, helium, oxygen, nitrogen, trifluoromethane, and sulfur hexafluoride.
FY 1997	Measure gas decomposition and ion energy distributions in inductively coupled plasmas.
FY 1998	Extend mass spectrometric diagnostics to rf plasmas in the presence of silicon wafers and transfer technique to industry.

2. Investigations of surface-charging in plasma processing

FY 1994	Observed effects of surface charging on ion energies in rf plasmas; Initiated compilation of surface-charge related bibliography.
FY 1995	Demonstrated measurement of electric fields using optical techniques; Completed surface charging bibliography.
FY 1996	Discontinued project based upon review of industrial needs and upon conclusions of strategic plan for support of electric power utilities. Personnel reassigned to projects with greater need and impact.

3. Compilation and analysis of fundamental data for the semiconductor industry

FY 1995	Initiate investigation of known electron impact cross sections for carbon tetrafluoride (CF_4) and trifluorourethane (CHF_3).
FY 1996	Completed electron-impact investigation for CF_4 and CHF_3; Published comprehensive paper and made summary data publicly available on World-Wide Web; Measured electron attachment to Dichloro-difluoromethane (CCl_2F_2) molecules.
FY 1997	Extend cross section investigation to include electron impact cross sections for CCl_2F_2, perfluoroethane (C_2F_6), and perfluoropropane (C_3F_8); Prepare comprehensive papers and make summary data available on World Wide Web.
FY 1998	Extend electron-impact cross section review to chlorine fluorine (C_4F_8); Develop capability to measure electron attachment cross sections using crossed beam method.
FY 1999	Measure electron attachment cross sections for radicals and excited species using crossed beam method.